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OPERATION MANUAL

CONTENTS

UNITRON 2200 PERSONAL COMPUTER

The U-2200 is a CP/M™ compatible microcomputer. This manual covers the information on the configuration, installation and operation. The bibliography in APPENDIX A lists several references which may aid you in use of various languages and operating systems.

CHAPTER 1

INTRODUCTION:

The U-2200 system has two major parts: Computer chassis and detached keyboard. A coiled cable connects between them.

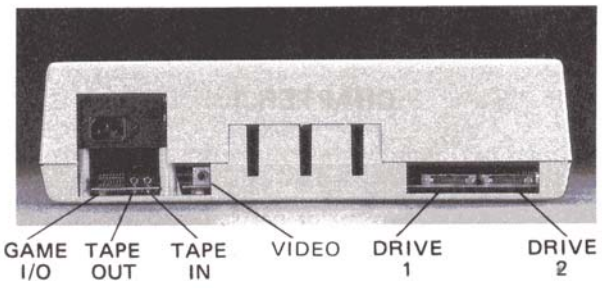
In this manual all descriptions of direction are based on your facing the machine, in FIG. 1-1.

FIG. 1-1

On the front of the chassis, as shown in FIG. 1-2, there are a power indicator and a keyboard connector.

FIG. 1-2 Front Panel

The rear panel has several connectors (Fig. 1-3) for Disk Drives, Video Monitor, Cassette Recorder and Joy stick.



The chassis contains the computerboard and power supply. Open the cover of chassis, and you will see the power supply on the right side above the computerboard. The power supply is a high frequency switching mode and provides four DC Voltages: +5V, +12V, −5V, −12V. The source of power can be either 110V AC or 220V AC, switch selectable (FIG. 1-4). The output of power supply connects to the computerboard via a 6-pin connector. The connector pinout is shown in Figure 1-5.

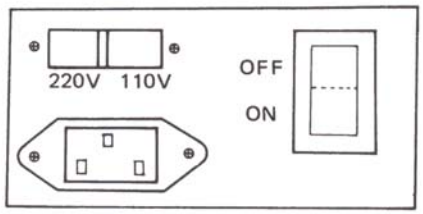


FIG. 1-4

GND	+12V	−5V	−12V	+5V	+5V

FIG. 1-5 Power Pinout

COMPUTERBOARD:

The U-2200 is a single board computer. The computerboard (Fig. 1-6) includes the 6502 and Z-80 microprocessors, RAM (Random Access Memory), ROM (Read only Memory), IC's (Integrated Circuits) and other components

required to make a functional computer. It also has 5 extention slots compatible with Apple II peripherals. These slots are numbered #1, #3, #4, #5 and #7.

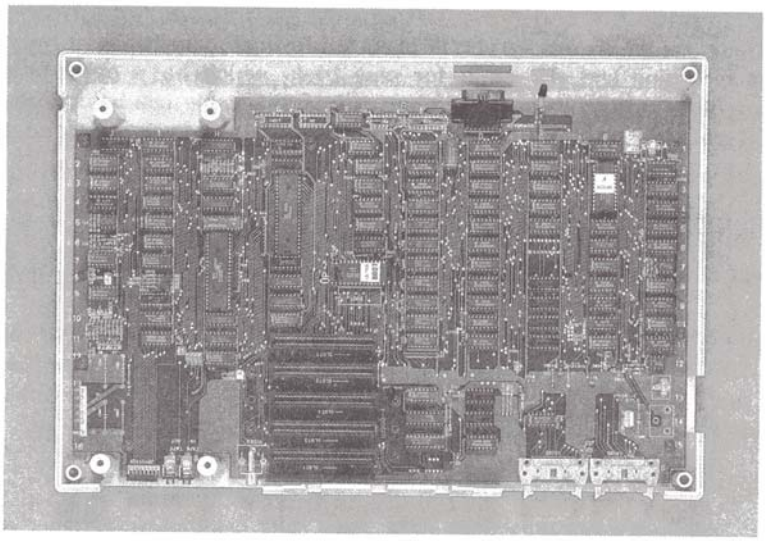


FIG. 1-6 Computerboard

VIDEO DISPLAY:

Display type:	Memory mapped display
Display mode:	Text, Low-resolution Graphics, High-Resolution Graphics.
Text capacity:	960 characters (24 lines, 40 columns)
Character type:	5x7 dot matrix
Character-set:	Upper/Lower case ASCII
Character modes:	Normal, Inverse, Flashing
Graphics capacity:	1920 blocks (Low-Resolution) in a 40 by 48 array.
	53760 dots (High-Resolution) in a 280 by 192 array.

In the center of rear side of the computerboard there is a metal connector marked "VIDEO". This connector allows you to attach a cable between the U-2200 and a closed-circuit video monitor. It is a female RCA phono jack. On the right rear conner, there is a 4-pin connector (ie. auxiliary video connector) for an RF modulator that can connect to either TV set or video mointor. The U-2200 has video soft-switch functions. If you have an 80-column card plugged in slot #3, you can plug the output of an 80-column video into a 2-pin Connector marked "80-col input" giving you automatic video switching.

THE CASSETTE INTERFACE:

On the right of the rear edge of computerboard are two small black packages labeled "Tape in" and "Tape out".

These are miniature earphone jacks into which you can plug two cables, one for recording and the other for play back, which has a pair of miniature earphone plugs on each end. The other end of this cable can be connected to a standard cassette tape recorder so that your U-2200 can save information on audio cassette tape and read it back again.

THE DISK DRIVE CONNECTORS:

The U-2200 computerboard includes the disk controller's functions which made by the advanced technology of PAL(TM) sequencer, so you can directly connect two drives. The connectors are located at the rear left of the computerboard. This controller (in dedicated slot #6) can drive two 5¼" floppy disk drives. If you wish to use more than two disk drives, plug extra disk interface cards in extention slots and connect drives as you need.

THE GAME I/O CONNECTOR:

To the right of cassette connectors is a 16-pin socket for game I/O. The purpose of the Game I/O connector is to connect special input and output devices to enhance the effect of programs, especially in game programs. This connector allows you to connect three one-bit inputs, four one-bit outputs, a data strobe, and four analog inputs, all of which can be managed by your programs.

KEYBOARD:

The U-2200 has a detached keyboard which connects to the computerboard with a coiled cable by a 15-pin female connector. Most of your contact with U-2200 will be through the keyboard. In the keyboard case there is an 8 ohm speaker controlled by a soft-switch. This soft-switch is associated with memory location number 49200. Any reference to this address (or the equivalent address −16336 or hexadecimal $C030H) will cause the speaker to emit a click.

Keyboard

Number of Keys: 72
Coding: Upper/Lower case ASCII
Output: Seven bits plus strobe
Power requirements: +5V at 300 MA
Special key: Numeric Keypad and
function keys

FIG. 1-7 Keyboard

VIDEO MONITOR

To operate the U-2200 system, you will also need a video monitor or a TV set. If you do not have a monitor and your TV set does not have a video input, you will need an RF modulator to modulates the video output signal on a standard TV channel frequency for display on a TV receiver. Remember, when a television is used, the quality of the display will not be as good as the display on a video monitor.

CHAPTER 2

INSTALLATION:

There are four connections you must make. They are power, video output, keyboard, and disk drive. They are normally made on the computer rear panel.

The power supply is 110/220V AC selectable, check your power source and set the switch to suit. The power receptacle is located in the upper right corner. Insert the end of the supplied power cord into this connector.

Video output is provided at either the RCA connector or the 4-pin connector for RF modulator. If a normal video monitor is being used, it can connect to the RCA connector or the video output of an RF modulator. If you use a TV set, connect it to the RF output of an RF modulator.

The keyboard has a coiled cable ended with a 15-pin D-type connector. Plug this connector to the male connector on the front panel.

On the left rear of the computerboard are two 20-pin connectors for disk drives. Connect your master drive in the connector labeled "drive 1".

If the 80-column card is used, plug it into slot #3, and the video output of the 80-column card connects to the 2-pin connector on the right of slot #7. The U-2200 provides an auto-switching function between 80/40 character Text display.

If a printer is used, plug the printer interface card into slot #1. Other cards can be plugged into any empty slots according to their instruction manuals.

GETTING STARTED

The U-2200 is a dual processor computer system. Both the 6502 and Z-80 microprocessors are supported for full, compatible operation in one computer.

Turn the power on after set-up. You will hear a "beep" from the speaker. The screen will show the message in FIG. 2-1.

UNITRON DUAL PROCESSORS COMPUTER SYSTEM
WITH AUTO-BOOTING CP/M.

CONNECT DISK DRIVE IN DRIVE 1 CONNECTOR
AND INSERT CP/M SYSTEM DISKETTE.

PRESS ANY KEY TO START!

FIG. 2-1

If there is no response or something strange happens, please turn the power off and check the following:

1: Keyboard connector and its direction.
2: Power connector and power source switch.
3: Video connector and 80-column video if installed.
4: Peripheral cards in slots.
5: Disk drive connections.

make sure every connection is correct, then turn the power on again. If it still does not work, press "control-reset" or check the connections again.

Once the correct message appears on the screen, insert the CP/M system diskette into drive 1 and press any key to boot CP/M.

If a message appears as FIG. 2-2, it means that the computer can not find the disk controller. You can press any key to try again.

*****CAN NOT FIND DISK CONTROLLER.**
PRESS ANY KEY TO RETRY

FIG. 2-2

The U-2200 has one ROM on the computerboard. This ROM is a booter. It boots the system from diskette.

The U-2200 has 24K ROM space split into two banks, switched by soft-switches. Refererring the address $C0A0 will switch to bank 1, address $C0AF to bank 0. You can add a ROM CARD for your applicatons.

CHAPTER 3

U-2200 OPERATION

The U-2200 is a dual processor computer. Both the 6502 and Z-80 microprocessors are supported for full, compatible operation in one computer. All circuitry except the power supply is located on a single computerboard.

TIMING

System timing is derived from the 14.318 MHZ crystal located at A1 on the computerboard.

Table 3-1 Timing Signals

SIGNAL	DESCRIPTION
14M	Master oscillator output. Used to derive other timing signals.
7M	7.159MHz timing signal.
ϕ0	1.023 MHZ phase 0 system clock. Complement to ϕI. Sometimes referred to as ϕ2 in other literature.
ϕ1	1.023 MHZ phase 1 system clock.
Q3	General purpose timing signal. Twice the frequency of the system clocks, but asymmetrical.

The video control and addressing signals are also generated by this circuitry. Video generation consists of 192 scan lines on the video screen. These are grouped into 24 lines of eight scan lines each. Fifteen synchronization signals are used. They consist of "H" (Horizontal) and "V" (Vertical) groups of signals. The V0 through V4 signals are used to define the vertical line position on the screen. The Va through Vc signals are used to define the vertical scan line position within the vertical screen line.

MEMORY

Memory in U-2200 consists of Random Access Memory (RAM), Read-only Memory (ROM), and I/O locations. The memory map is shown as Fig. 3-2. The RAM memory range $D000-$FFFF can be accessed like a language card. ROM space is 24K and is split into 2 banks. Softswitches are used to select the Bank 0 or Bank 1 ROM area. (Table 3-2). Power-on initialization is in bank 0.

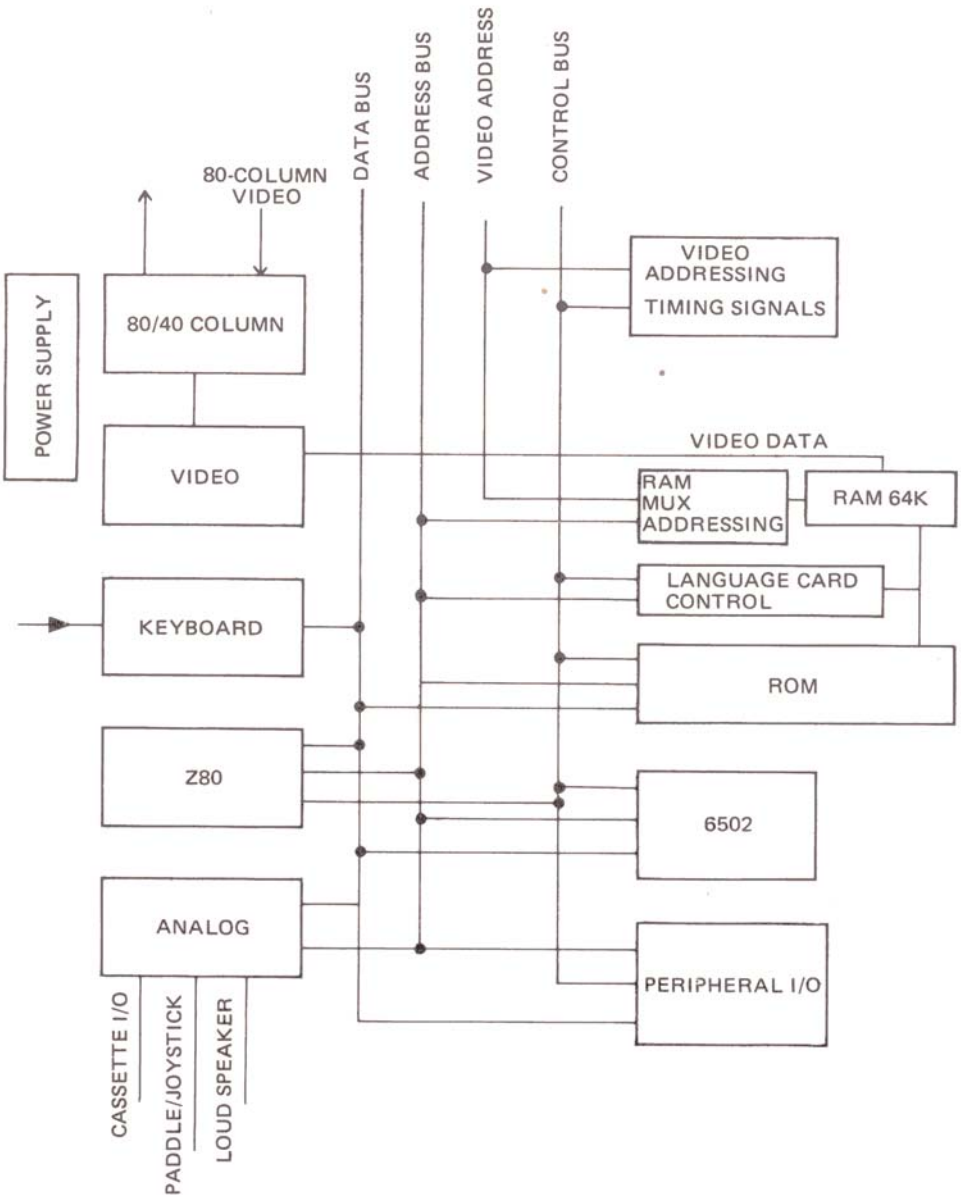


FIG. 3-1 System Block Diagram

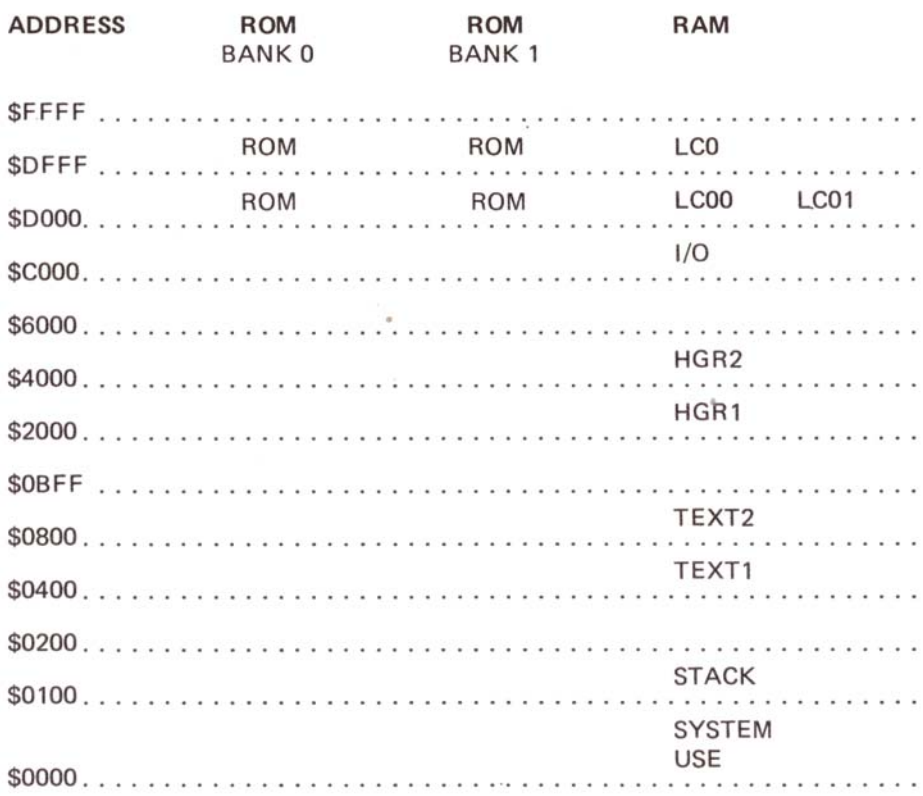


FIG. 3-2 System Memory Map

Table 3-2 Soft Switch Address for ROM Selection

	BANK 0	BANK 1
Address	$C0AF	$C0A0

LANGUAGE CARD AREA:

The upper 16K of RAM appears as a Language card. Soft switches are used to enable and disable ROM and RAM in this address range and are effective for whichever bank of ROM is selected. The architecture is such that there are two 4K block of RAM in the $D000-$DFFF memory range.

The system uses eight 4164 dynamic RAM's located in positions E4-E11. In location F8, there is 28-pin socket for ROM space. This will accept the 24-pin

booter ROM, aligmented at the bottom, which will boot CP/M. It will also accept the ROM CARD to use the 24K ROM space. The socket pinout is shown in Fig 3-5. Table 3-6 is the description of the signals.

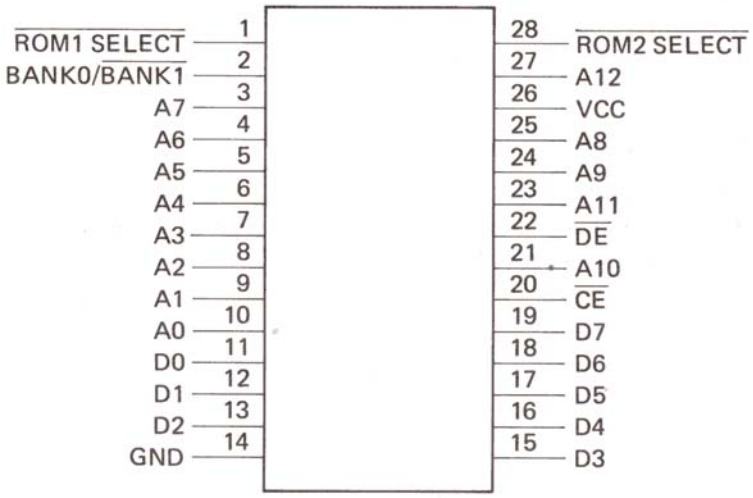


FIG. 3-5

Table 3-6

Signals	Description
ROM1 SELECT	Active Lo when the address is $F000-$FFFF of BANK 1.
ROM2 SELECT	Active Lo when the address is $D000-$EFFF of both banks.
CE, DE	Active Lo when the address is $F000-$FFFF of bank 0. The Booter ROM is enabled by this two signals.
BANK 0/BANK 1	Hi when in Bank 0. Lo when is Bank 1.
A0-A12	Address Bus.
D0-D7	Data Bus.

6502

The 6502 is a dynamic microprocessor operating at 1.023 MHz clock rate. It uses the address and data busses only when the $\phi 0$ signal is high or active. When $\phi 0$ is low, the microprocessor is doing internal operations and does not need the address and data busses.

Z-80

The Z-80 microprocessor is located on the computer board and is buffered to the address and data busses. The Z-80 is configured to allow direct execution of 8080 and Z-80 programs and operate under the CP/M operating system. The computer supports a 56K CP/M configuration.

TIMING

The Z-80 is synchronized and phase locked to the 6502 clocks. During the video refresh period, $\phi 1$, the 7 MHZ clock is divided into three half clock periods of 135 nanoseconds. The first half-clock is high, the second is low, and the third is high. At the end of the third half clock the signal goes low and remains low until the start of the next $\phi 1$. Thus, the Z-80 clock is low during all of $\phi 0$ and a small part of $\phi 1$. This timing scheme creates an effective Z-80 clock rate of 2.041 MHZ.

Each type of machine cycle contains one memory access period during $\phi 0$. The read/write signal is synchronized ensuring that the write can only go low during the time the Z-80 clock is high. Because all address transitions from the Z-80 occur when the clock is high, they must all occur during $\phi 1$ while the video update access is occurring. Thus, each $\phi 0$ has stable addresses on the bus for the entire duration of the cycle.

CONTROL

The Z-80 is controlled by write commands to the area of memory that normally contains a peripheral ROM. It is necessay to use write commands to ensure that the 6502 will not perform two accesses in succession, which would prevent switching back to the 6502.

When the U-2200 power is turned on, the RESET signal forces the Z-80 to the off state. The RESET signal is synchronized to the system clock to ensure that a write operation cannot be interrupted. The Z-80 is immediately placed in the WAIT mode and remains in this mode until activated.

Upon receipt of a write to the $C200-$C2FF area, the Z-80 is enabled. The Z-80 remains in the wait mode until one memory cycle occurs with Z-80 address informaton on the bus. At this point the Z-80 is allowed to run with no further wait cycles required. Receipt of another write to the $C200-$C2FF area of memory, by the Z-80, will return the Z-80 to the WAIT mode.

ADDRESS BUS INTERFACE

The Z-80 address bus interface is constructed such that the memory conflicts that exist between the 6502 based system and conventions used by the Z-80 microprocessor and CP/M are resolved. Table 3-7 shows how memory appears to the Z-80 versus normal 6502 configuration.

Table 3-7

Z-80 address	6502 address
$0000 – $0FFF	$1000 – $1FFF
$1000 – $1FFF	$2000 – $2FFF
$2000 – $2FFF	$3000 – $3FFF
$3000 – $3FFF	$4000 – $4FFF
$4000 – $4FFF	$5000 – $5FFF
$5000 – $5FFF	$6000 – $6FFF
$6000 – $6FFF	$7000 – $7FFF
$7000 – $7FFF	$8000 – $8FFF
$8000 – $8FFF	$9000 – $9FFF
$9000 – $9FFF	$A000 – $AFFF
$A000 – $AFFF	$B000 – $BFFF
$B000 – $BFFF	$D000 – $DFFF
$C000 – $CFFF	$E000 – $EFFF
$D000 – $DFFF	$F000 – $FFFF
$E000 – $EFFF	$C000 – $CFFF
$F000 – $FFFF	$0000 – $0FFF

Note that the Z-80 can address contiguous memory from $0000-$DFFF, without accessing the 6502's Zero page of memory or the peripheral I/O memory area.

PERIPHERAL I/O

Along the rear side of the computerboard are five peripheral I/O connectors. These connectors are used for peripheral interface boards designed for the U-2200 or the Apple II Computer. Peripheral Board I/O space has been set aside for use with each of the five slots and there is also a 2K common area for use by any of the boards installed.

Each of the slots is numbered. They are #1, #3, #4, #5 and #7. Each of the five 50-pin connectors is individually selected by control circuitry. Table 3-8 provides detail on the signals available at these connectors. The pinout is shown in FIG. 3-6.

Table 3-8 peripheral I/O signal descriptions

PIN	SIGNAL	DESCRIPTION
1	$\overline{\text{I/O SELECT}}$	This signal is normally high. It becomes low during $\phi 0$ when a reference is make to $CnXX, where 'n' is the slot number.
2-17	A0-A15	The buffered address bus. The address on these pins becomes valid through $\phi 0$.
18	R/W	Buffered Read/Write signal. This signal become valid the same time the address bus does, and goes high during a read cycle and low during a write cycle.
20	$\overline{\text{I/O STROBE}}$	Normally high, this line goes low during $\phi 0$ when the address bus contains an address between $C800 and $CFFF.
21	RDY	The 6502's RDY input. This signal is going low during $\phi 1$ halts the 6502 with the address bus holding the address of the current location being fetched.
22	$\overline{\text{DMA}}$	Pulling this line low disables the 6502's address bus and halts the 6502. The line is held high by a 1K ohm resistor to +5V.
23	INT OUT	Daisy-chain interrupt output to lower priority devices. This pin is usually connected to pin 28 (INT IN).
24	DMA OUT	Daisy chain DMA output to lower priority devices. This pin is usually connected to pin 27 (DMA IN).
25	+5V	+5V volt power supply. 3 Amps is available for use at the peripheral slots.
26	GROUND	System electrical ground.
27	DMA IN	Daisy-chain DMA input from higher priority devices. Usually connected to pin 24.
28	INT IN	Daisy-chain interrupt input from higher priority devices. Usually connected to pin 23 (INT OUT).

29	$\overline{\text{NMI}}$	Non-Maskable Interrupt. When this line is pulled low the U-2200 begins an interrupt cycle.
30	$\overline{\text{IRQ}}$	Interrupt Request. When this line is pulled low the U-2200 begins an interrupt cycle if 6502's interrupt disable (I) flag is not set.
31	$\overline{\text{RES}}$	When this line is pulled low the 6502 begins a RESET cycle.
32	$\overline{\text{INH}}$	This line is a input signal from peripheral cards. When this line is pulled low the ROM address range of $D000-$FFFF is disabled on the slots.
33	−12V	−12 volt power supply, 0.5 Amps is available for all peripheral slots.
34	−5V	−5 volt power supply, 0.5 Amps is available for all peripheral slots.
36	7M	7 MHZ clock.
37	Q3	Asymmetrical 2 MHZ clock.
38	ϕ1	Phase 1 clock.
39	USER 1	When this line is pulled low, all $C0XX-C7XX address decoding is inhibited.
40	ϕ0	Phase 0 clock.
41	$\overline{\text{DEVICE SELECT}}$	This signal becomes active — low, on a connector when the address bus holds an address between $C0n0 and $c0nF, where 'n' is the slot number plus $8.
42-49	D0-D7	Buffered bidirectional data bus. The data on these lines become valid 300 nsec into ϕ0 on a write cycle, and should be stable no less than 100 nsec before the end of ϕ0 on a read cycle.
50	+12V	+12 volot power supply, 2.5 Amps is available for all peripheral slots.

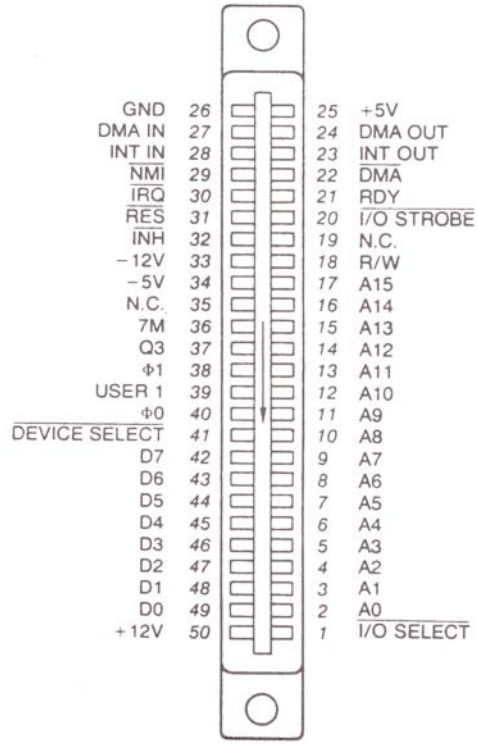


FIG. 3-6 Peripheral Connector Pinout

CHAPTER 4

VIDEO

SCREEN FORMAT

Three different kinds of information can be shown on the video display to which your U-2200 is connected (without 80-column card);

1) Text. U-2200 can display 24 lines of numbers, special symbols, and upper/ lower case letters with 40 of these characters on each line. These characters are formed in a dot matrix 7 dots high and 5 dots wide. There is a one-dot wide space on either side of the character and a one-dot high space above each line.

2) Low-Resolution Graphics. The U-2200 can present 1,920 squares in an array 40 blocks wide and 48 blocks high.

3) High-Resolution Graphics. The U-2200 can also display a dot matrix of 280 dots wide by 192 dots high.

SCREEN MEMORY

The video display uses information in the system's RAM to generate its display. The value of a single memory location controls the appearance of a particular fixed object on the screen. This object can be a character, two stacked blocks, or a line of seven dots. In Text and Low-Resolution Graphics mode, an area of memory containing 1024 locations is used as the source of the screen information. Text and Low-Resolution Grahics share this memory area. In High Resolution Graphics mode, a separate, larger area (8,192 locations) is needed because of the greater amount of information which is being displayed. These areas of memory are usually called "pages".

SCREEN PAGES

There are actually two areas from which each mode can draw its information. The first area is called the "primary page" or "page 1". The second area is called the "secondary page" or "page 2" and is an area of the same size immediately following the first area.

The secondary page is useful for storing pictures or text which you want to be able to display instantly. A program can use the two pages to perform animaion by drawing on one page while displaying the other and suddenly flipping pages.

Text and Low-Resolution Graphics share the same memory range for the secondary page, just as they share the same range for the primary page. Both mixed modes which were described above are also available on the secondary page, but there is no way to mix the two pages on the same screen.

VIDEO DISPLAY MEMORY RANGE

Screen	Page	Begins at: Hex	Dec	Ends at: Hex	Dec
Text/Lo-Res	Primary	$400	1024	$7FF	2047
	Secondary	$800	2048	$BFF	3071
Hi-Res	Primary	$2000	8192	$3FF	16383
	Secondary	$4000	16384	$5FF	24575

SCREEN SWITCHED

The devices which decide between the various modes, pages, and mixes are called "softswitches". They are switches because they have two positions (for example: on or off, text or graphics) and they are called "soft" because they are controlled by the software of the computer. A program can "throw" a switch by referencing the special memory location for that switch. The data which are read from or written to the location are irrelevant; it is the reference to the address of the location which throws the switch.

There are eight special memory locations which control the setting of the soft switches for the screen. They are set up in pairs; when you reference one location of the pair you turn its corresponding mode "on" and its companion mode "off". The pairs are:

Screen Soft Switches

Location:

Hex	Decimal		Description
$C050	49232	−16304	Display a GRAPHICS mode
$C051	49233	−16303	Display TEXT mode
$C052	49234	−16302	Display all TEXT or GRAPHICS
$C053	49235	−16301	Mix TEXT and a GRAPHICS mode
$C054	49236	−16300	Display the Primary page
$C055	49237	−16299	Display the Secondary page
$C056	49238	−16298	Display LO-RES GRAPHICS mode
$C057	49239	−16297	Display HI-RES GRAPHICS mode

ASCII SCREEN CHARACTERS

	Inverse				Flashing				(Control)		Normal				Lowercase)	
Decimal	0	16	32	48	64	80	96	112	128	144	160	176	192	208	224	240
Hex	$00	$10	$20	$30	$40	$50	$60	$70	$80	$90	$A0	$B0	$C0	$D0	$E0	$F0
0 $0	@	P		0	@	P		0	@	P		0	@	P		P
1 $1	A	Q	!	1	A	Q	!	1	A	Q	!	1	A	Q	a	q
2 $2	B	R	"	2	B	R	"	2	B	R	"	2	B	R	b	r
3 $3	C	S	#	3	C	S	#	3	C	S	#	3	C	S	c	s
4 $4	D	T	$	4	D	T	$	4	D	T	$	4	D	T	d	t
5 $5	E	U	%	5	E	U	%	5	E	U	%	5	E	U	e	u
6 $6	F	V	&	6	F	V	&	6	F	V	&	6	F	V	f	v
7 $7	G	W	'	7	G	W	'	7	G	W	'	7	G	W	g	w
8 $8	H	X	(	8	H	X	(	8	H	X	(	8	H	X	h	x
9 $9	I	Y	)	9	I	Y	)	9	I	Y	)	9	I	Y	i	y
10 $A	J	Z	*	:	J	Z	*	:	J	Z	*	:	J	Z	j	z
11 $B	K	[	+	;	K	[	+	;	K	[	+	;	K	[	k	{
12 $C	L	/	,	<	L	/	,	<	L	/	,	<	L	/	l	/
13 $D	M	]	-	=	M	]	-	=	M	]	-	=	M	]	m	}
14 $E	N	^	.	>	N	^	.	>	N	^	.	>	N	^	n	~
15 $F	O	-	/	?	O	-	/	?	O	-	/	?	O	-	o	rub

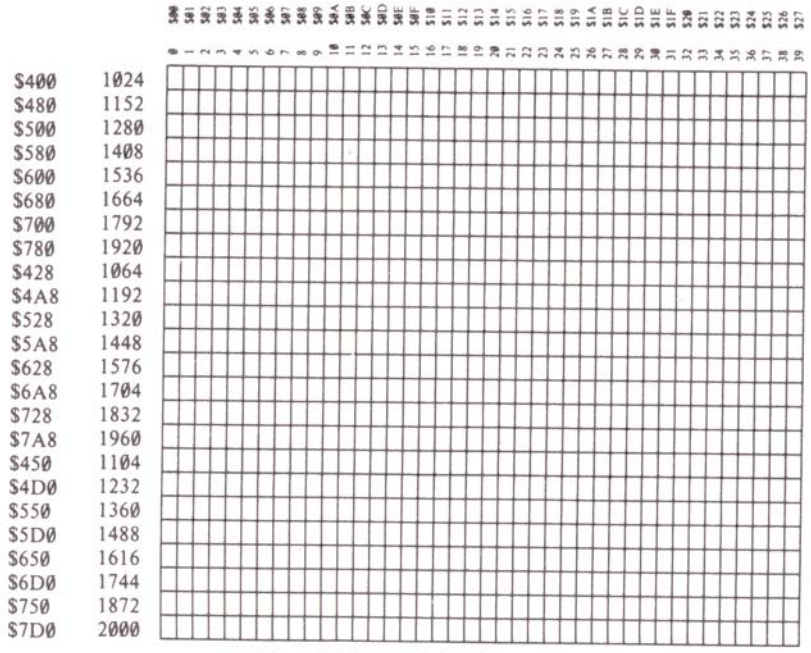


FIG. 4-1 Map of the Text screen

The TEXT Mode

In the Text mode, the U-2200 can display 24 lines of characters with up to 40 characters on each line. Each character on the screen represents the contents of one memory location from the memory range of the page being displayed. The character set includes the 26 upper-case letters, the 26 lower-case letters, the 10 digits, and 33 special characters.

The area of memory which is used for the primary text page starts at location number 1024 and extends to location number 2047. In machine language, the primary page is from hexadeciaml address $400 to address $7FF; the secondary page is from $800 to $BFF. Each of these pages is 1024 bytes long. Those of you intrepid enough to do the multiplication will realize that there are only 960 characters displayed on the screen. The remaining 64 bytes in each page which are not displayed on the screen are used as temporary storage by programs stored in PROM on interface peripheral boards.

Figure 4-1 is a map of the U-2200 display in text mode, with the memory location addresses for each character position on the screen.

THE LOW-RESOLUTION GRAPHICS (LO-RES) MODE

In the Low-Resolution Graphics mode, the U-2200 presents the contents of the same 1024 location of memory as for the Text mode, but in a different format. In this mode, each byte of memory is displayed not as an ASCII character, but as two blocks, stacked one atop the other. The screen can show an array of blocks 40 wide and 48 high, each block can be white or black.

Since each byte in the page of memory for Low-Resolution Graphic represent two blocks on the screen, stacked vertically, each byte is divided into two equal sections, called "nibbles". Each nibble can hold a value from zero to 15. The value which is in the lower nibble of the byte determines the color for the upper block of that byte on the screen, and the value which is in the lower nibble determines the color for the lower block on the screen. Value 0 is black, the others are white.

Figure 4-2 is a map of the U-2200's display in Low-Resolution Graphics mode, with the memory location addresses for each block on the screen.

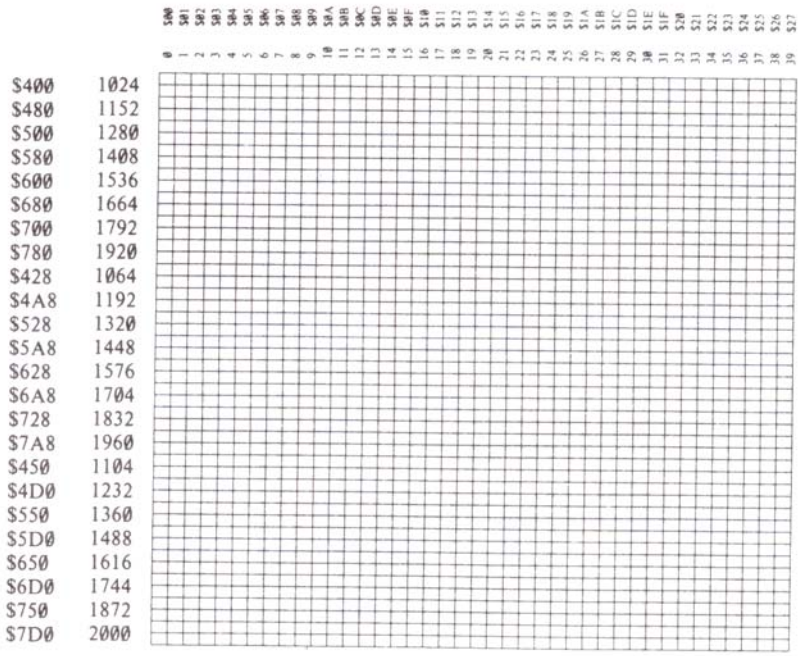


FIG. 4-2 Map of Low-Resolution Graphics Mode

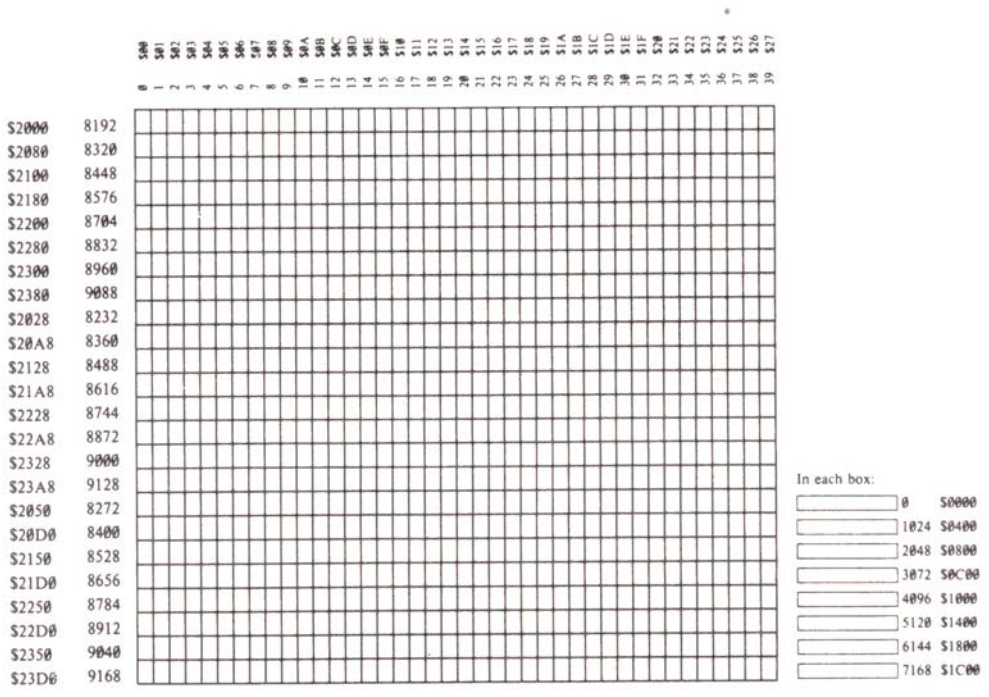


FIG. 4-3 Map of the High-Resolution Graphics Screen

THE HIGH-RESOLUTION GRAPHICS (HI-RES) MODE

The U-2200 has a second type of graphic display, called High-Resolution Graphics. When your U-2200 is in the High Resolution Graphics mode, it can display 53,760 dots in a matrix 280 dots wide and 192 dots high. The screen can display black and white dots.

The High-Resolution Graphics mode takes its data from an 8,192-byte area of memory, usually called a "picture buffer". There are two separate picture buffers: one for the primary page and one for the secondary page. Both of these buffers are independent of and separate from the memory areas used for Text and Low-Resolution Graphics. The primary page picture buffer for the High-Resolution Graphic mode begins at memory location number 8192 and extends up to location number 16384; the secondary page picture buffer follows on the heels of the first at memory location number 16384, extending up to location number 24575.

Each dot on the screen represents one bit from the picture buffer. Seven of the eight bits in each byte are displayed on the screen. Forty bytes are displayed on each line of the screen. The least significant bit (first bit) of the first byte in the line is displayed on the left edge of the screen., followed by the second bit, then the third, etc. The most significant (eighth) bit of each byte is not displayed. After one byte then follows the first bit of the next byte, and so on. A total of 280 dots are displayed on each of the 192 lines of the screen.

The dots whose corresponding bits are "on" (or equal to 1) appear white; the dots whose corresponding bits are "off" (or equal to 0) appear black. Figure 4-3 shows the U-2200's display screen in High-Resolution Graphics mode with the memory addresses of each line on the screen.

80-COLUMN SOFTSWITCH

The U-2200 has an 80-col video Auto-switching function worked by two soft-switches. Referencing the addresses $C051 and $C059 will switch to 80 column Text display if you have the 80-col card in its slot. Referencing the address $C058 or $C050 will return to 40 column display. Most CP/M software will search for the 80-column card and automatically switch to 80-col display if the card is found.

CHAPTER 5 INPUT/OUTPUT

The U-2200 has several built-in Input and Output (I/O) capabilities. Details of these I/O features are found in the remainder of this chapter.

. Keyboard
. Disk I/O
. Speaker
. Cassette I/O
. Game I/O

READING THE KEYBOARD

The keyboard sends seven bits of information which together form one character. These seven bits, along with another signal which indicates when a key has been pressed, are available to most programs as the contents of a memory location. When you press a key on the keyboard, the value in this location becomes 128 or greater, and the particular value it assumes is the numeric code for the character which was pressed. Table 5-1 shows the ASCII characters and their associated numeric codes. The location will hold this one value until you press another key, or until your program tells the memory location to forget the character it's holding.

Once your program has accepted and understood a keypress, it should tell the keyboard's memory location to "release" the character it is holding and prepare to receive a new one. Your program can do this by referencing another memory location. When you reference this other location, the value contained in the first location will drop below 128. This value will stay low until you press another key. This action is called "clearing the keyboard strobe". Your program can either read or write to the special memory location; the data which are written to or read from that location are irrelevant. Once you have cleared the keyboard strobe, you can still recover the code for the key which was last pressed by adding 128 ($80) to the value in the keyboard location.

These are the special memory locations used by the keyboard:

KEYBOARD SPECIAL LOCATIONS

Location			**Description**
Hex	**Decimal**		
$C000	49152	−16384	Keyboard Data
$C010	49168	−16368	Clear Keyboard Strobe

Table 5-1 The ASCII Character Set

Decimal:	Hex:	128 $80	144 $90	160 $A0	176 $B0	192 $C0	208 $D0	224 $E0	240 $F0
0	$0	nul	dle		0	@	P		p
1	$1	soh	dcl	!	1	A	Q	a	q
2	$2	stx	dc2	"	2	B	R	b	r
3	$3	etx	dc3	#	3	C	S	c	s
4	$4	eot	dc4	$	4	D	T	d	t
5	$5	enq	nak	%	5	E	U	e	u
6	$6	ack	syn	&	6	F	V	f	v
7	$7	bel	etb	'	7	G	W	g	w
8	$8	bs	can	(	8	H	X	h	x
9	$9	ht	em	)	9	I	Y	i	y
10	$A	lf	sub	*	:	J	Z	j	z
11	$B	vt	esc	+	;	K	[	k	{
12	$C	ff	fs	,	<	L	/	l	/
13	$D	cr	gs	—	=	M	]	m	
14	$E	so	rs	.	>	N	^	n	}
15	$F	si	us	/	?	O	—	o	rub

Table 5-2 Keys and their associated ASCII codes
Upper case Mode

Key	Alone	CTRL	SHIFT	Both	Key	Alone	CTRL	SHIFT	Both
space	$A0	$A0	$A0	$A0	RETURN	$8D	$8D	$8D	$8D
0	$B0	$B0	$C0	$C0	G	$C7	$87	$C7	$87
1!	$B1	$B1	$A1	$A1	H	$C8	$88	$C8	$88
2"	$B2	$B2	$A2	$A2	I	$C9	$89	$C9	$89
3#	$B3	$B3	$A3	$A3	J	$CA	$8A	$CA	$8A
4$	$B4	$B4	$A4	$A4	K	$CB	$8B	$CB	$8B
5%	$B5	$B5	$A5	$A5	L	$CC	$8C	$CC	$8C
6&	$B6	$B6	$A6	$A6	M	$CD	$8D	$CD	$8D
7'	$B7	$B7	$A7	$A7	N	$CE	$8E	$CE	$8E
8(	$B8	$B8	$A8	$A8	O	$CF	$8F	$CF	$8F
9)	$B9	$B9	$A9	$A9	P@	$D0	$90	$D0	$90
*	$BA	$BA	$AA	$AA	Q	$D1	$91	$D1	$91
;+	$BB	$BB	$AB	$AB	R	$D2	$92	$D2	$92
,<	$AC	$AC	$BC	$BC	S	$D3	$93	$D3	$93
-=	$AD	$AD	$BD	$BD	T	$D4	$94	$D4	$94
.>	$AE	$AE	$BE	$BE	U	$D5	$95	$D5	$95
/?	$AF	$AF	$BF	$BF	V	$D6	$96	$D6	$96
A	$C1	$81	$C1	$81	W	$D7	$97	$D7	$97
B	$C2	$82	$C2	$82	X	$D8	$98	$D8	$98
C	$C3	$83	$C3	$83	Y	$D9	$99	$D9	$99
D	$C4	$84	$C4	$84	Z	$DA	$9A	$DA	$9A
E	$C5	$85	$C5	$85	←	$88	$88	$88	$88
F	$C6	$86	$C6	$86	→	$95	$95	$95	$95
					ESC	$9B	$9B	$9B	$9B
					^]	$DE	$9E	$DD	$9D

Lower case Mode

	Alone	Shift		Alone	Shift
A	E1	C1	M	ED	CD
B	E2	C2	N	EE	CE
C	E3	C3	O	EF	CF
D	E4	C4	P	F0	D0
E	E5	C5	Q	F1	D1
F	E6	C6	R	F2	D2
G	E7	C7	S	F3	D3
H	E8	C8	T	F4	D4
I	E9	C9	U	F5	D5
J	EA	CA	V	F6	D6
K	EB	CB	W	F7	D7
L	EC	CC	X	F8	D8
			Y	F9	D9
			Z	FA	DA

The U-2233 Keyboard has many predefined and user-defined function keys and each key has autorepeat function. The operation will be found in Keyboard operation sheet.

The RESET key at the upper right corner of the main section does not generate an ASCII code, but instead is directly connected to the microprocessor. When the RESET and CTRL keys are pressed together, all processing stops. When the key is released, the computer starts a reset cycle.

The CTRL and SHIFT keys generate no codes by themselves, but only alter the codes produced by other keys.

The power light at the lower left-hand corner is an indicator lamp to show when the power is on. This key is also a switch to set a flip-flop for upper/lower case characters.

DISK I/O

The U-2200 has two disk I/O connectors on the rear panel. The booter will boot CP/M from the drive 1 connector. Table 5-3 lists the pin out of the connector which is compatible with Apple disk drives.

Table 5-3

pin	description
1, 3, 5, 7	GROUND
2	Q0
4	Q1
6	Q2
8	Q3
9	−12V
10	WR REQ
11, 12	+5V
13, 15, 17, 19	+12V
14	ENABLE
16	READ DATA
18	WRITE DATA
20	WRITE PROTECTION

SPEAKER

Inside the keyboard case, there is a small 8 ohm speaker. It is connected to the internal electronics of the U-2200 so that a program can cause it to make a variety of sounds.

The speaker is controlled by a soft switch. This soft switch is not like the soft switches controlling the video modes, but is instead a toggle switch. Each time a program references the memory address associated with the speaker switch, the speaker will change state: change form "in" to "out" or vice-versa. Each time the state is changed, the speaker produces a tiny "click". By referencing the address of the speaker switch frequently and continuously, a program can generate a steady tone from the speaker.

The soft switch for the speaker is associated with memory location number 49200. Any reference to this address ($C030) will cause the speaker to emit a click.

CASSETTE I/O

There are two small black packages labelled "TAPE IN" and "TAPE OUT" for cassette I/O. The connector marked "out" is wired to another soft switch on the U-2200 board. This is another toggle switch, like the speaker switch. The soft switch for the cassette output plug can be toggled by referencing memory location number 49184 (or the equivalent −16352 or hexadecimal $C020). Referencing this location will make the voltage on the out connector swing from zero to 25 millivolts, or return from 25 millivolts back to zero. If the other end of the cable is plugged into the MICROPHONE input of the cassette tape recoder which is recording onto a tape, this will produce a tiny "click" on the tape. By repetition the program produces a tone on the tape. By varying the pitch and duration of this tone, information may be encoded data on a tape and saved for later use.

Be forewarned that if you attempt to flip the soft switch for the cassette output by writing to its special location you will actually generate two "clicks" on the recording. You should only use "read" operations when toggling the cassette output soft switch.

The other connector, marked "TAPE IN", can be used to "listen" to a cassette tape recording. Its main purpose is to provide a means of listening to tones on the tape, decoding them into data, and storing them in memory. Thus, programs or data which were stored on cassette tape may be read back and used again.

The input circuit takes a 1 volt (peak-to-peak) signal from the cassette recorder's EARPHONE jack and converts it into a string of ones and zeroes. Each time the signal is applied to the input circuit swings from positive to negative, or vice-versa, the input circuit changes state: if it was sending ones, it will start sending zeroes, and vice versa. A program can inspect the state of the cassette input circuit by looking at memory location number 29248 or the equivalents −16288 or hexadecimal $C060. If the value which is read from this location is greater than or equal to 128, then the state is a "one", if the value in the memory location is less than 128, then the state is a "zero". Although BASIC programs can read the state of the cassette input circuit, the speed of a BASIC program is usually much too slow to be able to make any sense out of what it reads.

GAME I/O

The purpose of the Game I/O connector is to allow you to connect special input and output devices to heighten the effect of programs in general, specifically game programs. The connector allows you to connect three one-bit inputs, four one-bit outputs, a data strobe, and four analog inputs to the U-2200, all of which can be controlled by your programs. The Game controllers connected to cables can plug into the Game I/O connector. The two rotary dials on the controllers are connected to two analog inputs on the connector. The two push buttons are connected to two of the one-bit inputs.

ANNUNCIATOR OUTPUTS

The four one-bit outputs are called "annunciators". Each annunciator output can be used as an input to some other electronic device, or the annunciator outputs can be connected to circuits to drive lamps, relays, speakers, etc.

Each annunciator is controlled by a soft switch. The addresses of the soft switch for the annunciators are arranged into four pairs, one pair for each annunciator. If you reference the first address in a pair, you turn the output of its corresponding annunciator "off", if you reference the second address in the pair, you turn the annunciator's output "on". When an annunciator is "off", the voltage on its pin on the Game I/O connector is near 0 volts; when an annunciator is "on", the voltage is near 5 volts. There is no inherent means to determine the current setting of an annunciator bit. The annunciator soft switches are:

TABLE 5-4 ANNUNCIATOR SPECIAL LOCATION

	Ann	State	Address Decimal	Hex
0	off	49240	−16296	$C058
	on	49241	−16295	$C059
1	off	49242	−16294	$C05A
	on	49243	−16293	$C05B
2	off	49244	−16292	$C05C
	on	49245	−16291	$C05D
3	off	49246	−16290	$C05E
	on	49247	−16289	$C05F

ONE-BIT INPUTS

The three one-bit inputs can each be connected to either another electronic device or to a pushbutton. You can read the state of any of the one-bit input from a machine language or BASIC program in the same manner as you read the Cassette Input Addresses 49249 through 49251 (16287 through −16285 or hexadeciaml $C061 through $C063).

ANALOG INPUTS

The four analog inputs can be connected to 150K ohm variable resistors or potentiometers. The variable resistance between each input and the +5 Volt supply is used in a one-shot timing circuit. As the resistance on an input varies, the timing characteristics of its corresponding timing circuit change accordingly. Machine language programs can sense the changes in timing loops and obtain a numerical value corresponding to the position of the potentiometer.

Before a program can start to read the setting of a potentiometer, it must first reset the timing circuits. Location number 49264 (−16272 or hexadeciaml $C070) does just this. When you reset the timing circuits, the values contained in the four locations 49252 through 49255 become greater than 128 (their high bits are set). Within 3.060 milliseconds, the values contained in these four locations should drop below 128. The exact time it takes for each location to drop in value is directly proportional to the setting of the game paddle associated with that location. If the potentiometers connected to the analog inputs have a greater resistance than 150K ohms, or there are no potentiometers connected, then the values in the game controller locations might never drop to zero.

STROBE OUTPUT

There is an additional output, called C040STROBE, which is normally +5 Volts but will drop to zero volts for a duration of one-half microsecond under the control of a machine language or BASIC program. You can trigger this "strobe" by referring to location number 49216 (−1632 or $C04F). Be aware that if you perform a "write" operation to this location, you will trigger the strobe twice.

TABLE 5-5: INPUT/OUTPUT SPECIAL LOCATIONS

Function	Address	Decimal	Hex	Read/Write
speaker	49200	−16336	$C030	R
cassette out	49184	−16352	$C020	R
cassette In	49256	−16288	$C060	R
Annunciators	49240	−16296	$C058	R/W
	through	through	through	
	49247	−16289	$C05F	
Flag inputs	49249	−16287	$C061	R
	49250	−16286	$C062	R
	49251	−16285	$C063	R
Analog	49252	−16284	$C064	R
inputs	49253	−16283	$C065	
	49254	−16282	$C066	
	49255	−16281	$C067	
Analog Clear	49264	−16272	$C070	R/W
Utility Strobe	49216	−16320	$C040	R

THE GAME I/O CONNECTOR

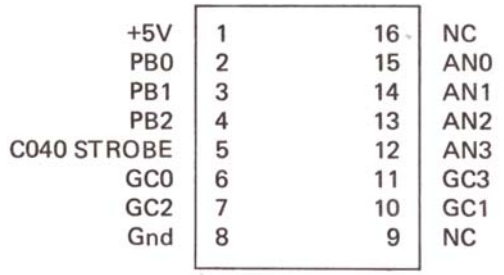


FIG. 5-1 Game I/O Connector Pinouts

Table 5-6 Game I/O Signal Descriptions

Pin:	Name:	Description:
1	+5V	+5 volt power supply. Total current drain on this pin must be less than 100mA.
2-4	PB0-PB2	Single-bit (Pushbutton) inputs. These are standard 74LS series TTL inputs.
5	C040 STROBE	A general-purpose strobe. This line, normally high, goes low during $\phi 0$ of a read or write cycle to any address from $C040 through $C04F. This is a standard 74LS TTL output.
6, 7, 10, 11	GC0-GC3	Game controller inputs. These should each be connected through a 150K Ohm variable resistor to +5v.
8	Gnd	System electrical ground.
12-15	AN0-AN3	Annunciator outputs. These are standard 74LS series TTL outputs and must be buffered if used to drive other than TTL inputs.
9, 16	NC	No internal connection.

APPENDIX A

REFERENCE

1. Apple II Reference Manual
   (product number A2L0001A)

2. Basic Programming Reference Manual
   (product number A2L0006)

3. Apple II Basic Programming Manual
   (product number A2L005X)

4. The DOS Manual
   (product number A2L0036)

5. Apple Pascal Operating System Manual
   (product number A2L0028)

6. 6502 Assembly Language Programming by Lance A. Leventhal

7. Programming The Z-80 by Rodnay Zaks

8. Softcard Manual

9. The CP/M Handbook with MP/M by Rodnay Zaks